MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

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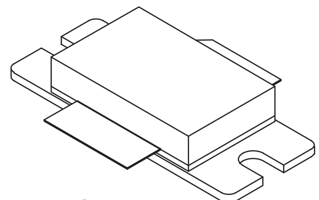
The RF Sub–Micron MOSFET Line
RF Power Field Effect Transistors
N–Channel Enhancement–Mode Lateral MOSFETs

MRF21125
MRF21125S
MRF21125SR3

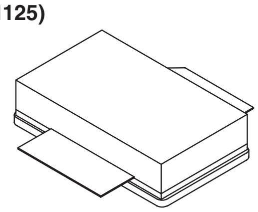
Designed for W–CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN–PCS/cellular radio and WLL applications.

- Typical 2–carrier W–CDMA Performance for V_{DD} = 28 Volts, I_{DQ} = 1600 mA, f1 = 2.1125 GHz, f2 = 2.1225 GHz, Channel bandwidth = 3.84 MHz, adjacent channels at ± 5 MHz , ACPR and IM3 measured in 3.84 MHz bandwidth. Peak/Avg = 8.5 dB @ 0.01% probability on CCDF.
  Output Power — 20 Watts
  Efficiency — 18%
  Gain — 13 dB
  IM3 — –43 dBc
  ACPR — –45 dBc
- 100% Tested under 2–carrier W–CDMA
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 28 Vdc, 2170 MHz, 125 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.

2170 MHz, 125 W, 28 V
LATERAL N–CHANNEL
RF POWER MOSFETs



CASE 465B–03, STYLE 1
(NI–880)
(MRF21125)



CASE 465C–02, STYLE 1
(NI–880S)
(MRF21125S)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	330 1.89	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.53	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 5

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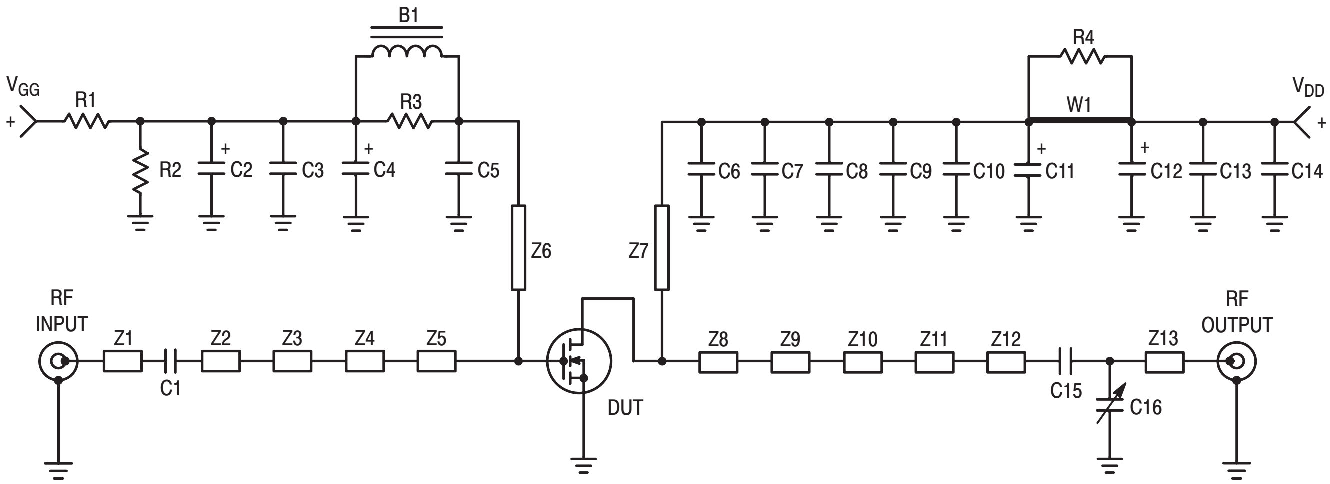
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 100 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
ON CHARACTERISTICS					
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 3 Adc)	g_{fs}	—	10.8	—	S
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 300 μA)	$V_{GS(th)}$	2	—	4	Vdc
Gate Quiescent Voltage (V_{DS} = 28 V, I_D = 1300 mA)	$V_{GS(Q)}$	2.5	3.9	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 1 A)	$V_{DS(on)}$	—	0.12	—	Vdc
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (1) (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	5.4	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture) 2–carrier W–CDMA, 3.84 MHz Channel Bandwidth, IM3 measured in 3.84 MHz Bandwidth. Peak/Avg = 8.5 dB @ 0.01% probability on CCDF.					
Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 20 W Avg, 2–carrier W–CDMA, I_{DQ} = 1600 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz)	G_{ps}	12	13	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 20 W Avg, 2–carrier W–CDMA, I_{DQ} = 1600 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz)	η	17	18	—	%
Third Order Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 20 W Avg, 2–carrier W–CDMA, I_{DQ} = 1600 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz; IM3 measured at f1 –15 MHz and f2 +15 MHz referenced to carrier channel power.)	IM3	—	–43	–40	dBc
Adjacent Channel Power Ratio (V_{DD} = 28 Vdc, P_{out} = 20 W Avg, 2–carrier W–CDMA, I_{DQ} = 1600 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz; ACPR measured at f1 –10 MHz and f2 +10 MHz referenced to carrier channel power.)	ACPR	—	–45	–40	dBc
Input Return Loss (V_{DD} = 28 Vdc, P_{out} = 20 W Avg, 2–carrier W–CDMA, I_{DQ} = 1600 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz)	IRL	—	–12	–9.0	dB
Output Mismatch Stress (V_{DD} = 28 Vdc, P_{out} = 125 W CW, I_{DQ} = 1600 mA, f = 2170 MHz, VSWR = 5:1, All Phase Angles at Frequency of Test)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
TYPICAL TWO–TONE PERFORMANCE (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 125 W PEP, I_{DQ} = 1600 mA, f1 = 2110 MHz, f2 = 2120 MHz and f1 = 2160 MHz, f2 = 2170 MHz)	G_{ps}	—	12	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 125 W PEP, I_{DQ} = 1600 mA, f1 = 2110 MHz, f2 = 2120 MHz and f1 = 2160 MHz, f2 = 2170 MHz)	η	—	34	—	%
Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 125 W PEP, I_{DQ} = 1600 mA, f1 = 2110 MHz, f2 = 2120 MHz and f1 = 2160 MHz, f2 = 2170 MHz)	IMD	—	–30	—	dBc
TYPICAL CW PERFORMANCE					
Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 125 W CW, I_{DQ} = 1600 mA, f1 = 2170.0 MHz)	G_{ps}	—	11.5	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 125 W CW, I_{DQ} = 1600 mA, f = 2170.0 MHz)	η	—	46	—	%



Z1	1.212″ x 0.082″ Microstrip	Z9	0.179″ x 0.219″ Microstrip
Z2	0.236″ x 0.082″ Microstrip	Z10	0.100″ x 0.336″ Microstrip
Z3	0.086″ x 0.254″ Microstrip	Z11	0.534″ x 0.142″ Microstrip
Z4	0.357″ x 0.082″ Microstrip	Z12	0.089″ x 0.080″ Microstrip
Z5	0.274″ x 1.030″ Microstrip	Z13	0.620″ x 0.080″ Microstrip
Z6	0.466″ x 0.050″ Microstrip	Raw Board Material	0.030″ Glass Teflon®, 2 oz Copper, 3″ x 5″ Dimensions, Arlon GX0300–55–22, ε_r = 2.55
Z7	0.501″ x 0.050″ Microstrip		
Z8	0.600″ x 1.056″ Microstrip		

Figure 1. MRF21125 Test Circuit Schematic

Table 1. MRF21125 Test Circuit Component Designations and Values

Designators	Description
B1	Ferrite Bead (Square), Fair Rite #2743019447
C1	9.1 pF Chip Capacitor, B Case, ATC #100B9R1CCA500X
C2, C4, C11, C12	22 μF, 35 V Tantalum Surface Mount Chip Capacitors, Kemet #T491X226K035AS4394
C3, C7	20000 pF Chip Capacitors, B Case, ATC #100B203JCA50X
C5, C14	5.1 pF Chip Capacitors, B Case, ATC #100B5R1CCA500X
C6	100000 pF Chip Capacitor, B Case, ATC #100B104JCA50X
C8	10000 pF Chip Capacitor, B Case, ATC #100B103JCA50X
C9	7.5 pF Chip Capacitor, B Case, ATC #100B7R5CCA500X
C10	1.2 pF Chip Capacitor, B Case, ATC #100B1R2CCA500X
C13	0.1 μF Chip Capacitor, Kemet #CDR33BX104AKWS
C15	16 pF Chip Capacitor, B Case, ATC #100B160KP500X
C16	0.6 – 4.5 pF Variable Capacitor, Johanson Gigatrim #27271SL
R1	1.0 kΩ, 1/8 W Chip Resistor
R2	560 kΩ, 1/8 W Chip Resistor
R3	4.7 Ω, 1/8 W Chip Resistor
R4	12 Ω, 1/8 W Chip Resistor
W1	Solid Copper Buss Wire, 16 AWG

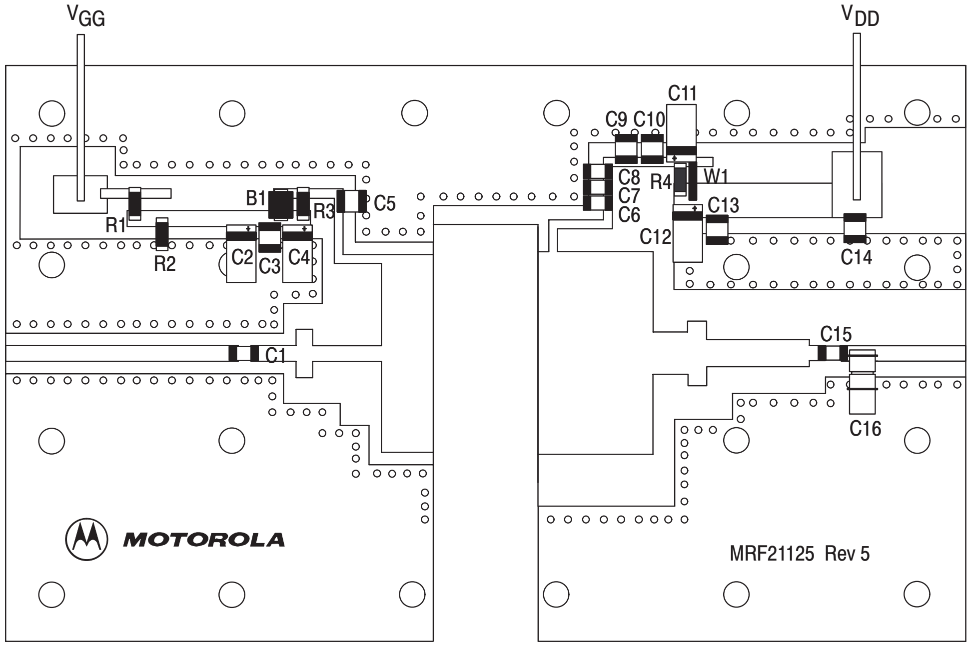


Figure 2. MRF21125 Test Circuit Component Layout

TYPICAL CHARACTERISTICS

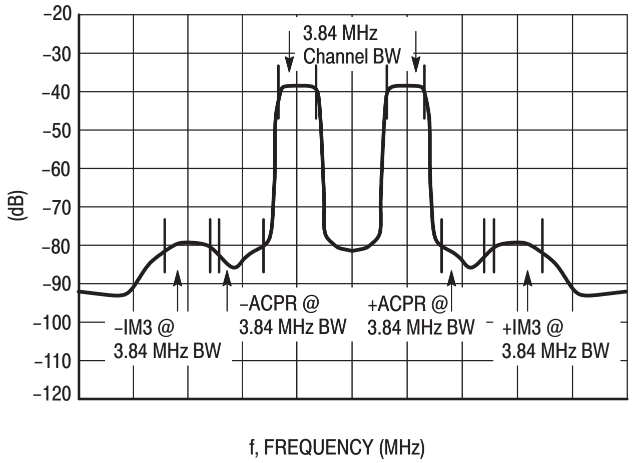


Figure 3. 2 Carrier (10 MHz spacing) W−CDMA Spectrum

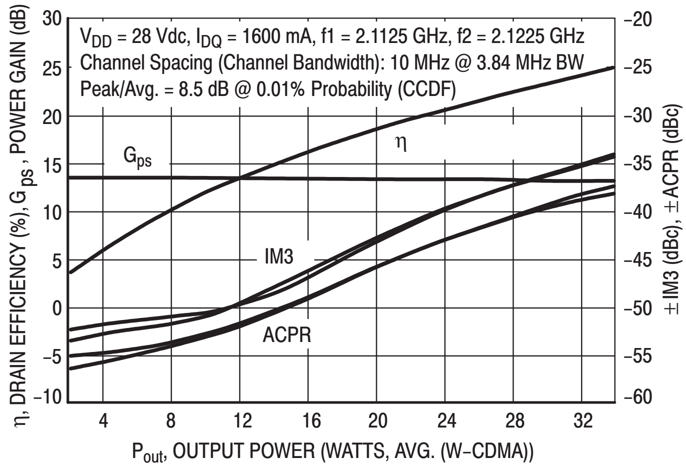


Figure 4. 2 Carrier W−CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power

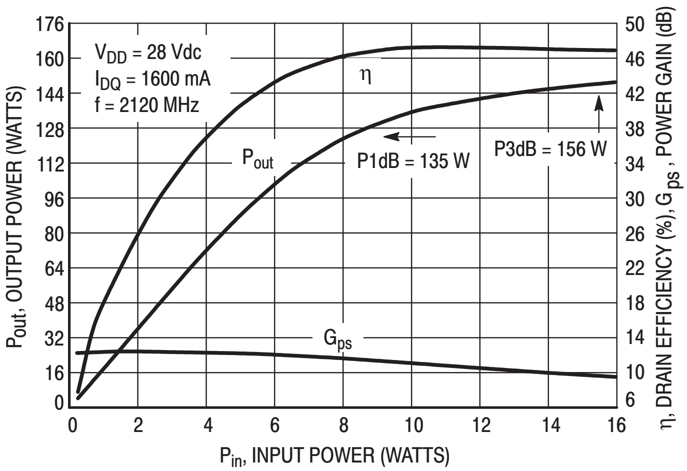


Figure 5. CW Performance

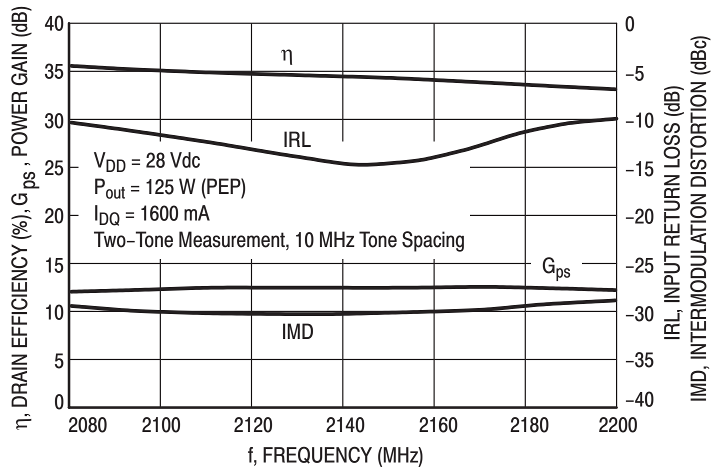


Figure 6. Broadband Linearity Performance

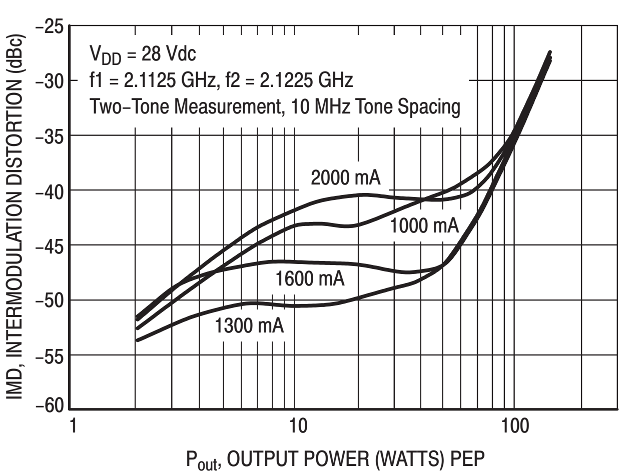


Figure 7. Intermodulation Distortion versus Output Power

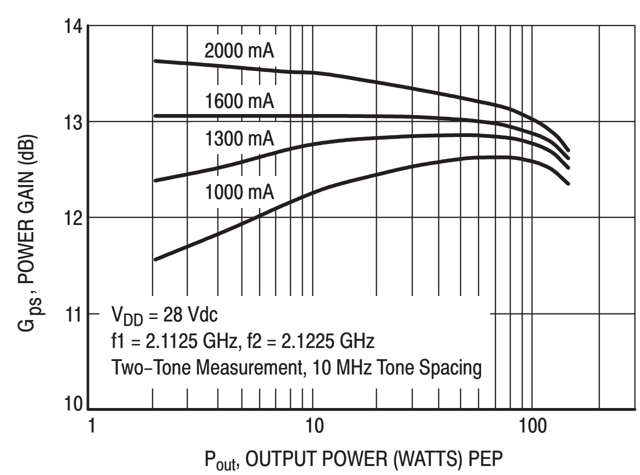
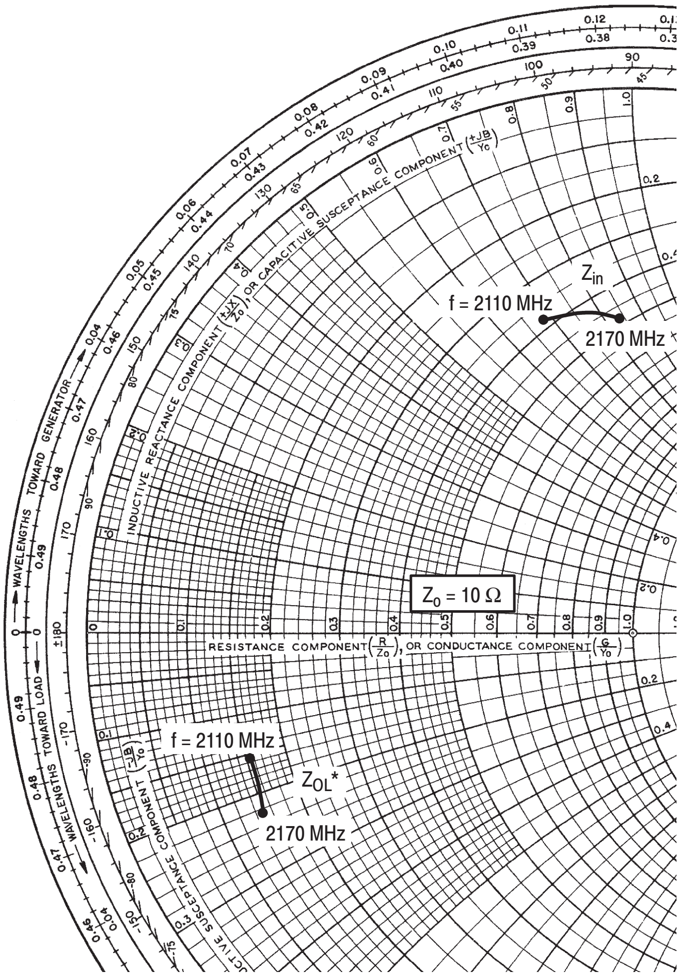


Figure 8. Power Gain versus Output Power



V_{DD} = 28 V, I_{DQ} = 1600 mA, P_{out} = 20 W (Avg.), 2−Carrier W−CDMA

f MHz	Z_{in} Ω	Z_{OL}* Ω
2110	3.81 + j6.86	1.56 – j1.58
2140	4.33 + j7.90	1.53 – j1.90
2170	4.84 + j8.46	1.48 – j2.26

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note 1: Z_{OL}* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

Note 2: Measurements were taken on the MRF21125 test circuit with SMA Launchers.

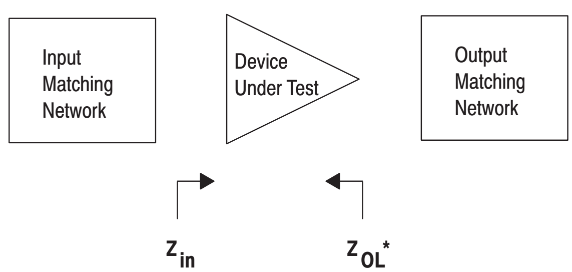


Figure 9. Series Equivalent Input and Output Impedance

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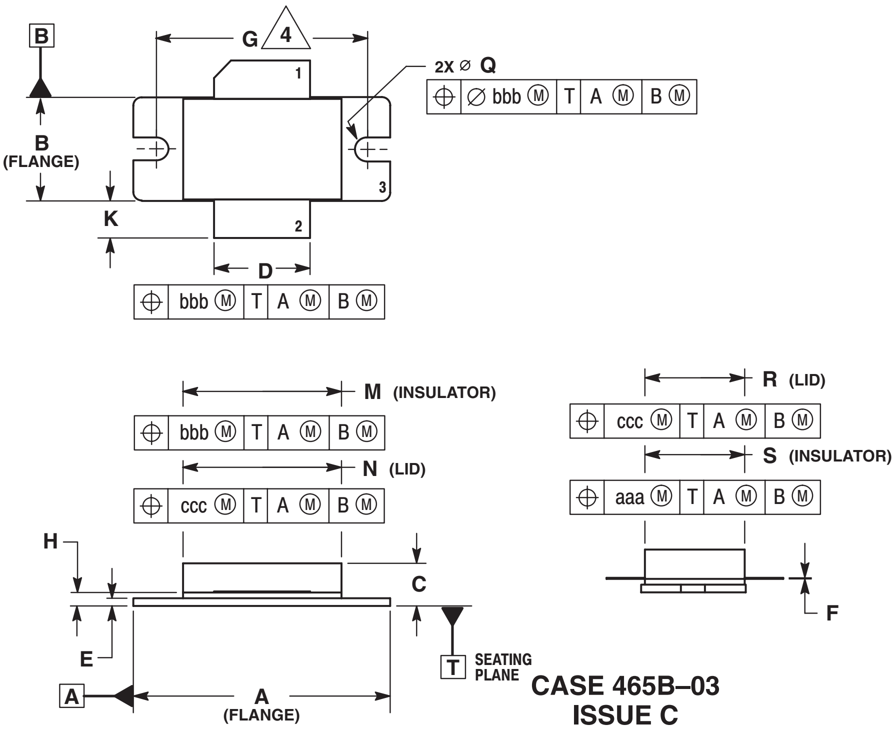
PACKAGE DIMENSIONS

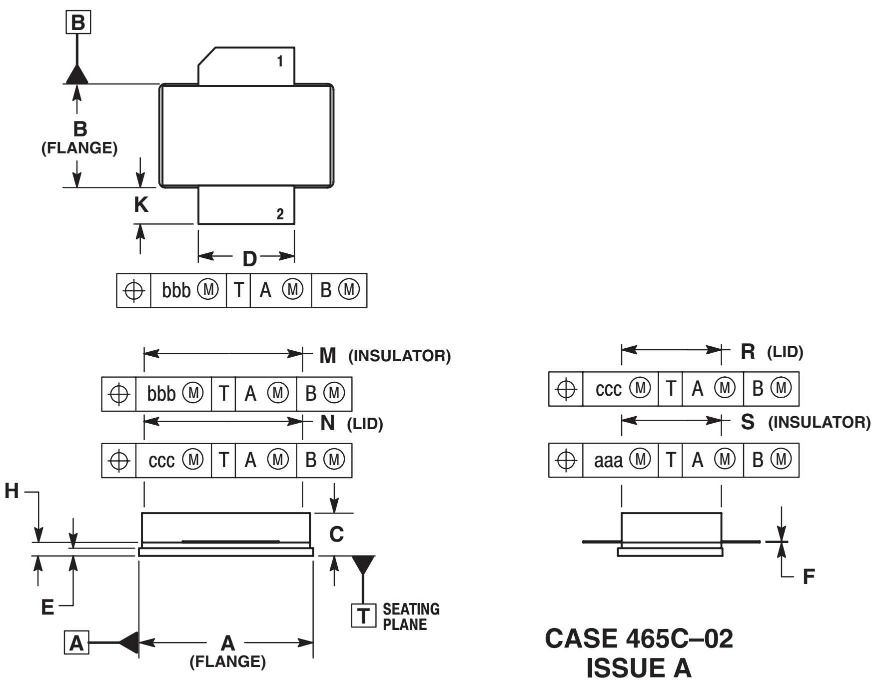


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.
4. RECOMMENDED BOLT CENTER DIMENSION OF 1.16 (29.57) BASED ON M3 SCREW.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.335	1.345	33.91	34.16
B	0.535	0.545	13.6	13.8
C	0.147	0.200	3.73	5.08
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.057	0.067	1.45	1.70
K	0.175	0.205	4.44	5.21
M	0.872	0.888	22.15	22.55
N	0.871	0.889	19.30	22.60
Q	⌀.118	⌀.138	⌀3.00	⌀3.51
R	0.515	0.525	13.10	13.30
S	0.515	0.525	13.10	13.30
aaa	0.007 REF		0.178 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465B–03
ISSUE C
(NI–880)
(MRF21125)



NOTES:
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2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.905	0.915	22.99	23.24
B	0.535	0.545	13.60	13.80
C	0.147	0.200	3.73	5.08
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.872	0.888	22.15	22.55
N	0.871	0.889	19.30	22.60
R	0.515	0.525	13.10	13.30
S	0.515	0.525	13.10	13.30
aaa	0.007 REF		0.178 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465C–02
ISSUE A
(NI–880S)
(MRF21125S)

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